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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,187	01/22/2004	Koichi Kishiro	OKI.628	2712

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EXAMINER	
NOVACEK, CHRISTY L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,187	KISHIRO, KOICHI	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/22/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the communication filed January 22, 2004.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "204" and "206" are shown as both pointing to the same thing in Figure 6.

The drawings are objected to because Figure 6 shows two different layers both being designated by the reference character "210".

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: "208" (Figure 6).

Figure 6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,214,722) in view of Ogure et al. (US 6,458,694).

Regarding claim 1, Lin discloses a wafer having a supporting body (200) and an intermediate insulating film (202) on the whole upper surface of the supporting body, removing a layered portion of the intermediate insulating film on the wafer edge region lying around the wafer by etching using a resist pattern (204a) to thereby expose an edge surface region of the supporting body which corresponds to the wafer edge region, and forming a conductive layer (220) that covers the exposed edge surface region and the upper side of the remaining intermediate insulating film (Fig. 2A-2F; col. 3, ln. 7-54). Lin discloses that the conductive layer may be a metal or polysilicon but does not disclose any particular method used for depositing this layer. Like Lin, Ogure discloses a method of forming metal interconnect layers within an interlayer dielectric layer of a semiconductor device. Ogure teaches that it is advantageous to deposit the metal interconnect layer by using a sputtering process because it provides a high deposition rate and excellent film quality (col. 1, ln. 38-46; col. 3, ln. 55 – col. 4, ln. 8). At the time of the invention, it would have been obvious to one of ordinary skill in the art to deposit the metal interconnect layer of Lin by the sputtering method taught by Ogure because Ogure discloses that sputtering provides the benefits of a high deposition rate and excellent film quality.

Regarding claim 2, Lin discloses that prior to etching using the resist pattern, a resist film is formed over the entire upper surface of the intermediate insulating film, a peripheral exposure function exposes a resist edge region corresponding to the wafer edge region and the resist edge region subjected to the peripheral exposure is removed (Fig. 2C-2D; col. 3, ln. 10-36).

Regarding claims 4 and 5, Lin does not specifically disclose that the supporting body is formed from a semiconductor material. Ogure discloses forming metal interconnections for an integrated circuit on a semiconductor wafer (Abstract). At the time of the invention, it would have been obvious to form the supporting body of Lin of a semiconductor material as is taught by Ogure because forming an integrated circuit on a semiconductor wafer is well-known and conventional in the art.

Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,214,722) in view of Ogure et al. (US 6,458,694) as applied to claim 1 above, and further in view of Wolf et al. ("Silicon Processing for the VLSI Era: Volume 1").

Regarding claim 3, Lin discloses that prior to etching using the resist pattern, a resist film is formed over the entire upper surface of the intermediate insulating film. Lin discloses that the resist is subjected to a development step but Lin does not disclose any particular development method (col. 3, ln. 30-36). Wolf discloses a development process for removing a photoresist region to be used as a pattern. The development process involves providing a fresh supply of developer chemicals onto the upper surface of the resist film by a spin-coating apparatus (pp. 445). At the time of the invention, it would have been obvious to one of ordinary skill in the art to conduct the development step of Lin as is taught by Wolf because Lin does not disclose any

particular development process and Wolf teaches that the spin-coating process can successfully be used to develop a resist pattern.

Regarding claim 6, Lin does not specifically disclose that the supporting body is formed from a semiconductor material. Ogure discloses forming metal interconnections for an integrated circuit on a semiconductor wafer (Abstract). At the time of the invention, it would have been obvious to form the supporting body of Lin of a semiconductor material as is taught by Ogure because forming an integrated circuit on a semiconductor wafer is well-known and conventional in the art.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Bao et al. (US 6,472,312) disclose depositing an insulating layer on a semiconductor substrate such that there is a lateral offset between the edge of the insulating layer and the edge of the substrate and depositing a conductive layer so as to cover the edge of the insulating layer.

Okada (US 6,242,337) discloses depositing an insulating layer on a semiconductor substrate, etching the insulating layer using a mask pattern such that there is a lateral offset between the edge of the insulating layer and the edge of the substrate and depositing a conductive layer so as to cover the edge of the insulating layer.

Wei et al. (US 5,966,628) disclose depositing an insulating layer on a semiconductor substrate, etching the insulating layer using a mask pattern such that there is a lateral offset between the edge of the insulating layer and the edge of the substrate and depositing a conductive layer so as to cover the edge of the insulating layer.

Shen et al. (US 5,723,385) disclose depositing an insulating layer on a substrate, etching the insulating layer such that there is a lateral offset between the edge of the insulating layer and the edge of the substrate and depositing a conductive layer so as to cover the edge of the insulating layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
April 14, 2005

Michael Trinh
Primary Examiner